

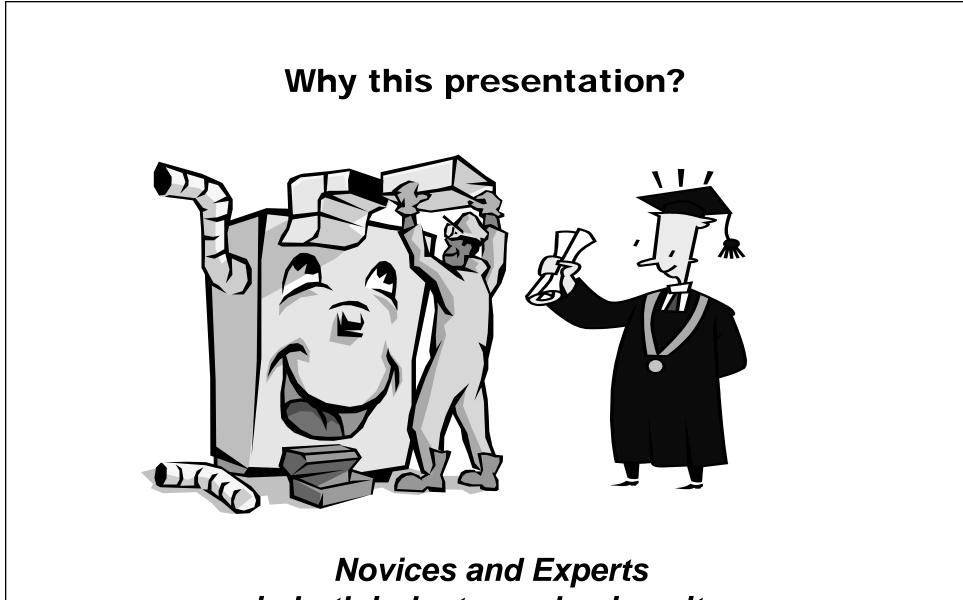
Most Common Mistakes with Real-Time Software Development

Embedded Systems Conference Boston, September 2006 Class ESC 401/421



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in both industry and university, make the same mistakes over and over again.

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The Order

The order is subjective, based on personal observations when using the following criteria:





How often is the mistake made?

Does the mistake increase complexity of the code?

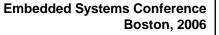
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What is the bottom line regarding Time and Money?

What is the effect of the mistake on reliability?



12345678910

The Order is Not Really Important What is important is that the mistake is on the list!

Correcting just ONE mistake can save thousands of dollars or significantly improve quality and robustness of software.



Correcting SEVERAL mistakes can lead to savings and improvements that are incalculable!

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"My Problem is Different"



Learn from experience of others

Focus on similarities, not differences

Rarely, if ever, is entire problem different



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Delays implemented as empty loops

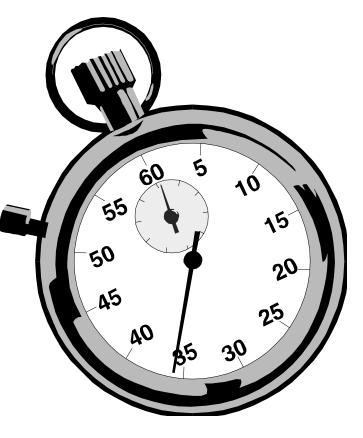


Use RTOS timing mechanisms

Build your own mechanism that automatically profiles CPU

Poll the count-down value of a timer

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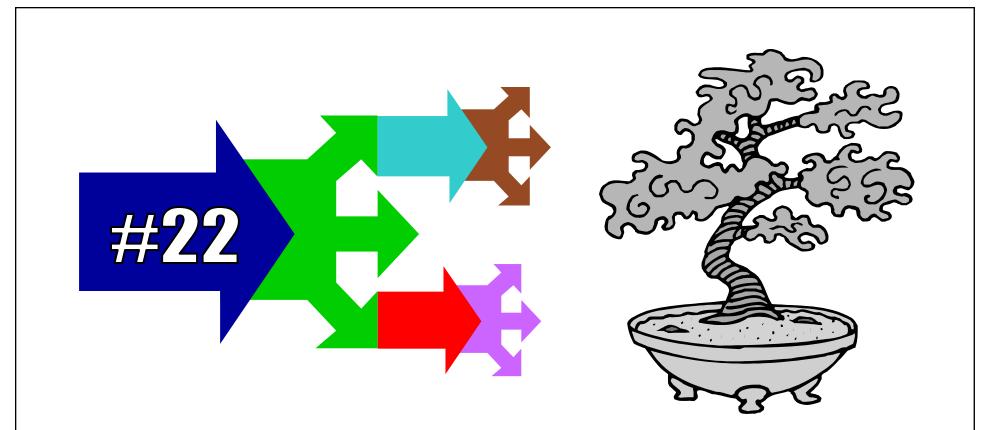


Tools choice driven by marketing hype, not by evaluation of technical needs

Select tools based on your own technical needs, not just because everybody else is using them.

Spending \$2,000 for the right tool can save \$100,000 in labor.

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Large *if-then-else* and *case* statements Usually a sign of implementation without design.

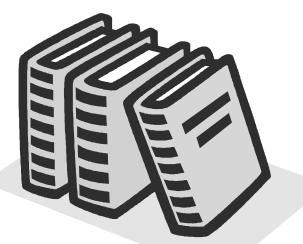
Instead, Design First! Use Finite State Machines to reduce complexity.

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Start implementation with documentation (the design document)

Revise documentation interactively; this serves as a sanity check to ensure that the code implements everything defined in it.

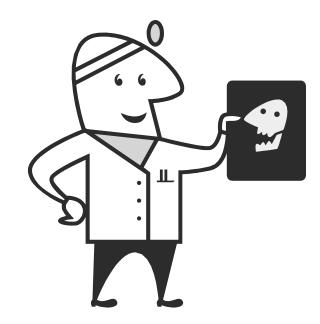
Document is written when functionality is fresh in programmer's mind.





Documentation written *after* implementation

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Interactive and incomplete test programs

Instead:

Create non-interactive test programs

Simulate input devices with known patterns

Always test the entire application all the time

Nightly extensive self-tests

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Software Engineers Don't Participate in Hardware Design



Leads to over-designing the system Instead, promote Hardware/Software Co-Design



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No Simulators of Target Application



Using a simulator:

Faster development Better debugging tools Multiple programmers Customer feedback Deeper understanding Safer and cheaper! Embedded Systems Conference

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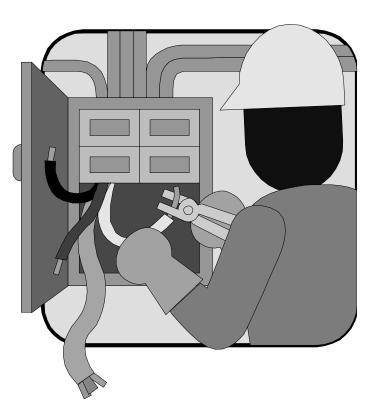
Boston, 2006

Error detection and handling is an after-thought, and implemented through trial and error



Treat errors as inputs, and error handling as a state

Error detection and handling must be specified and designed prior to implementation.

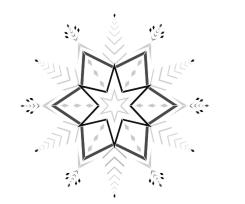


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Generalizations based on a single architecture





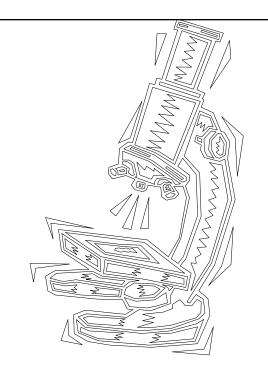
Develop code on multiple architectures simultaneously Don't generalize everything! Create configurable modules for whatever is different between architectures

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Optimizing at the Wrong Time

3*x or x+x+x



Do not perform fine-grain optimizations unless needed, and only during final stages of implementation

Measure performance after each optimization to ensure it is in fact an optimization

Do coarse-grain optimization during design phase

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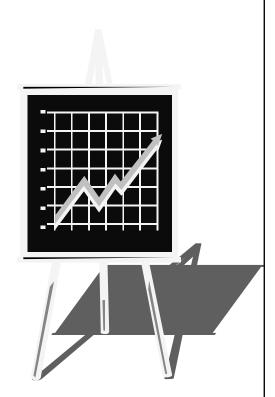
Optimizing at the Wrong Time

To perform good coarse-grain optimization, must analyze hardware peculiarities before starting

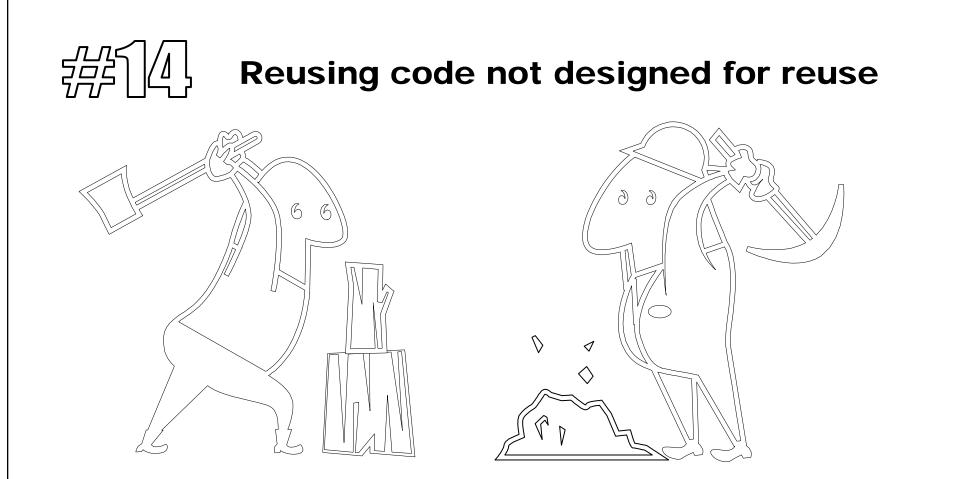
Profile CPU before writing programs for it, to identify and understand anomalies.

Better understanding of hardware peculiarities will lead to better designs.

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On a 9 MHz Z180:	
Byte+byte:	7 usec
16-bit+16-bit:	12 usec
32-bit+32-bit:	28 usec
float+float:	137 usec
float+byte:	308 usec



Don't waste time trying to use old code that was not designed for reuse. Instead, re-design it using proven techniques for software reuse.

Using blocking forms of message passing



Problems:

- Reduced real-time schedulable bound
- Significant overhead
- Results in lots of aperiodic servers
- Forces tight synchronization
- Potential for deadlock in closed-loop systems
- Additional complexity for 1:many communication

Schedulable bound: The maximum utilization of the processor for which a task set is guaranteed to still meet all its timing constraints. Ideally, schedulable bound is 100%. In practice, it is lower than that.

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Using blocking forms of message passing

Solution:

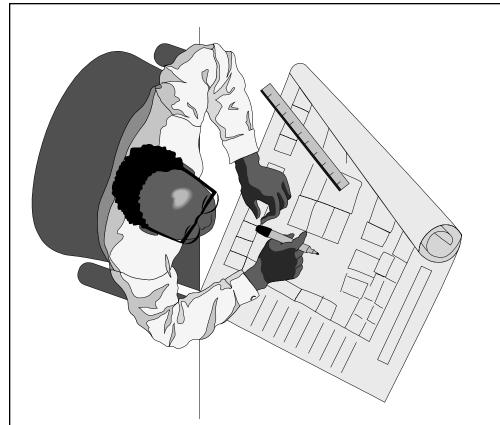
Minimize inter-module communication and synchronization

Use a shared-memory based protocol, such as state variable communication, publish/subscribe, or non-blocking message passing.

If blocking is unavoidable, use proper synchronization techniques to prevent priority inversion and deadlock, such as priority ceiling protocol.

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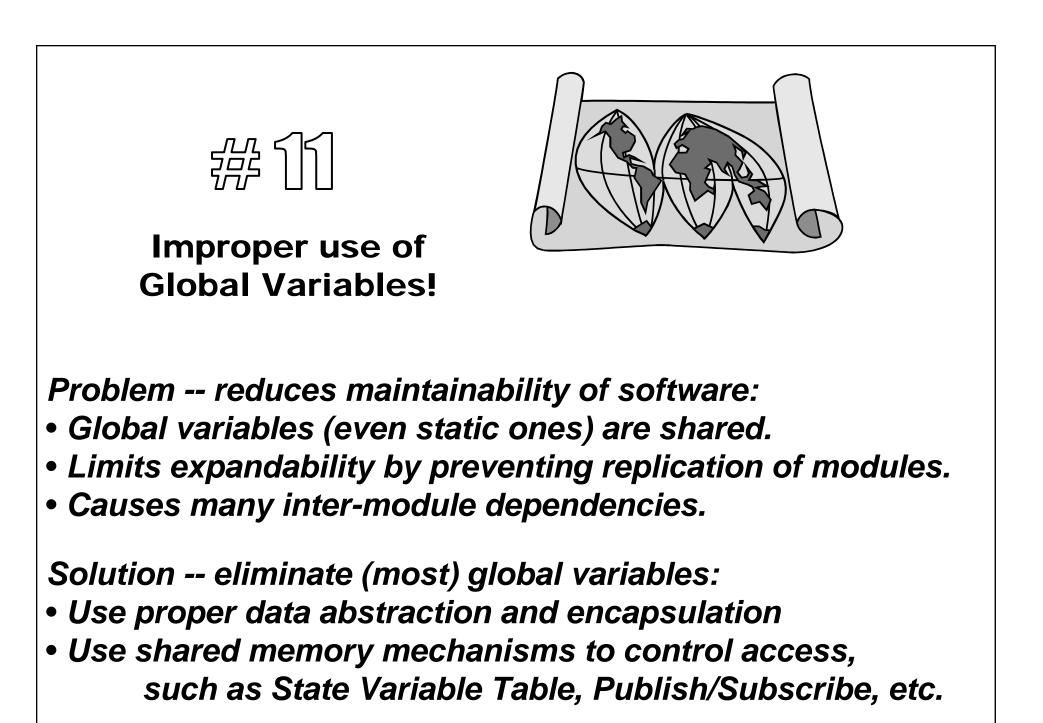
No memory analysis during design

Compute memory usage during design phase.

Don't forget about memory used by string constants.

For code, estimate a budget for each module.

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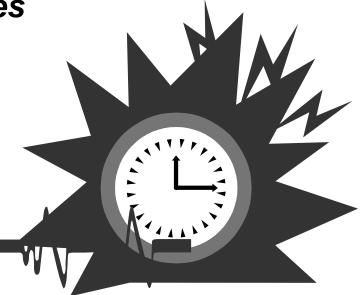


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Interrupts are an enemy to real-time predictability:

- Always have high priority
- Force a need for global variables
- Cannot be scheduled
- Difficult to analyze
- Execute within wrong context
- Operate in kernel space
- Priority inversion
- Difficult to debug



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Instead, minimize use of interrupts whenever possible

Periodic polling threads are more desirable than interrupts because they are schedulable

Complex code should be replaced by a signal to an aperiodic server

Only use real-time analysis methods that take interrupt handling into account

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Myth: Interrupts save CPU time over processes Reality: Not usually in real-time systems

Interrupts: 20 to 50 μ sec per interrupt Threads: 50 to 100 μ sec per context switch Non-preemptive processes: 10 to 30 μ sec per switch

A real-time executive with non-preemptive periodic processes can sometimes provide more predictable results and better utilization than using interrupts.

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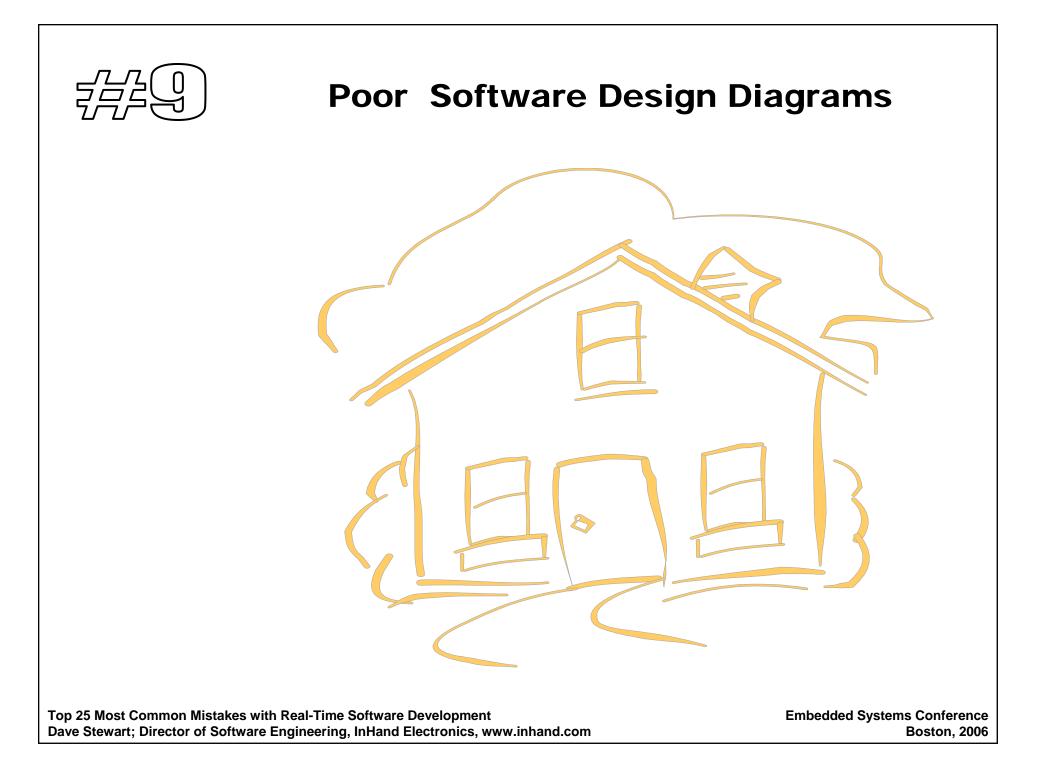


Myth: Interrupts save CPU time over processes Reality: Not usually in real-time systems

Interrupts save a bit of overhead, but at the huge cost of reducing the schedulable bound and increasing the possibility of race conditions

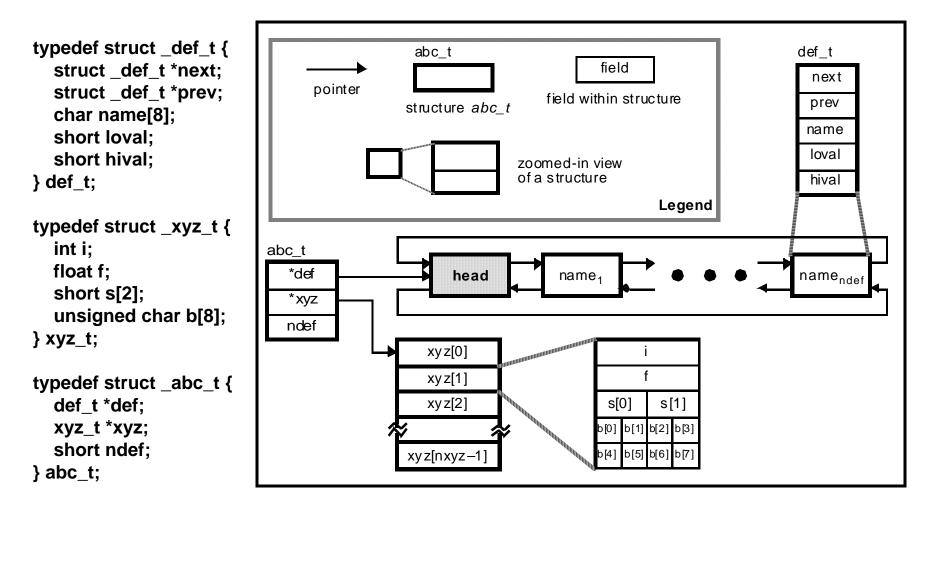
Saving 10% overhead by using interrupts might reduce schedulable bound by 30% and increase overhead of using shared variables by 20%!

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No Software Design Diagrams



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Architectural decomposition: at least one diagram per level of decomposition

Detailed design: at least one diagram per function or module

> Process-flow Data-flow Finite-state machines Dependency graphs Data relationships Sequence

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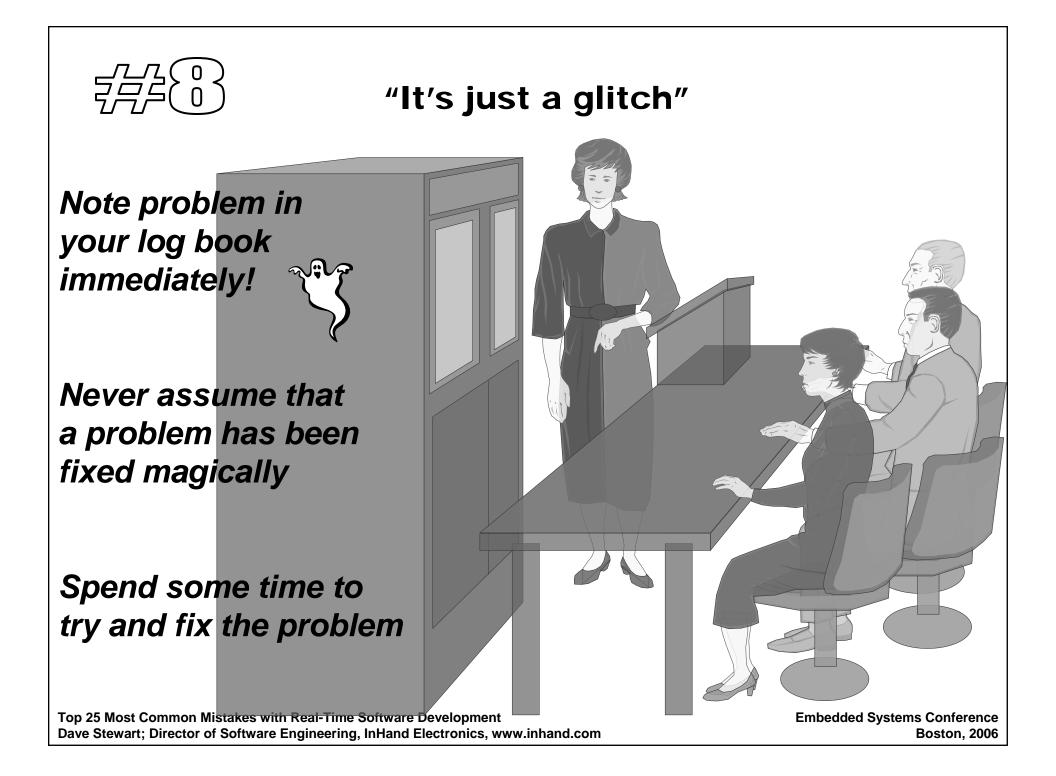
How do we create good diagrams?

Create a legend for every diagram.

Every block, symbol, line, shading, color, and font type should be specified in legend.

Any deviation from legend shows an error in the design.

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"It's just a glitch"

What are the most likely causes?

Timing Error (race condition, priority inversion) Memory Corruption Deadlock

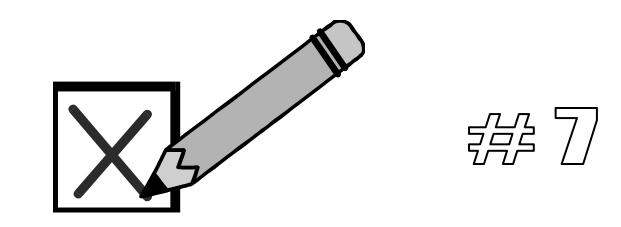


"It's just a glitch"

How do we pinpoint the problem?

(1) During design phase, take precautions: Formal code review Minimize shared resources and memory Minimize use of interrupts Use deadlock-free IPC solutions

(2) During testing and maintenance phases: Put sleep() commands within critical sections Check for stack corruption Incrementally add debug statements Monitor progress on logic analyzer



The first right answer is the only answer

Every problem has at least 3 answers: The first answer The opposite answer A compromise between the first two answers Which is the best answer?

Learn to be more creative to find the other answers.

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Studies have shown that more problems can get fixed in one day of code review than in a month of debugging

Reviews help eliminate messy code by forcing programmers to show their code to others

Reviews double as training sessions to increase number of employees who understand the code

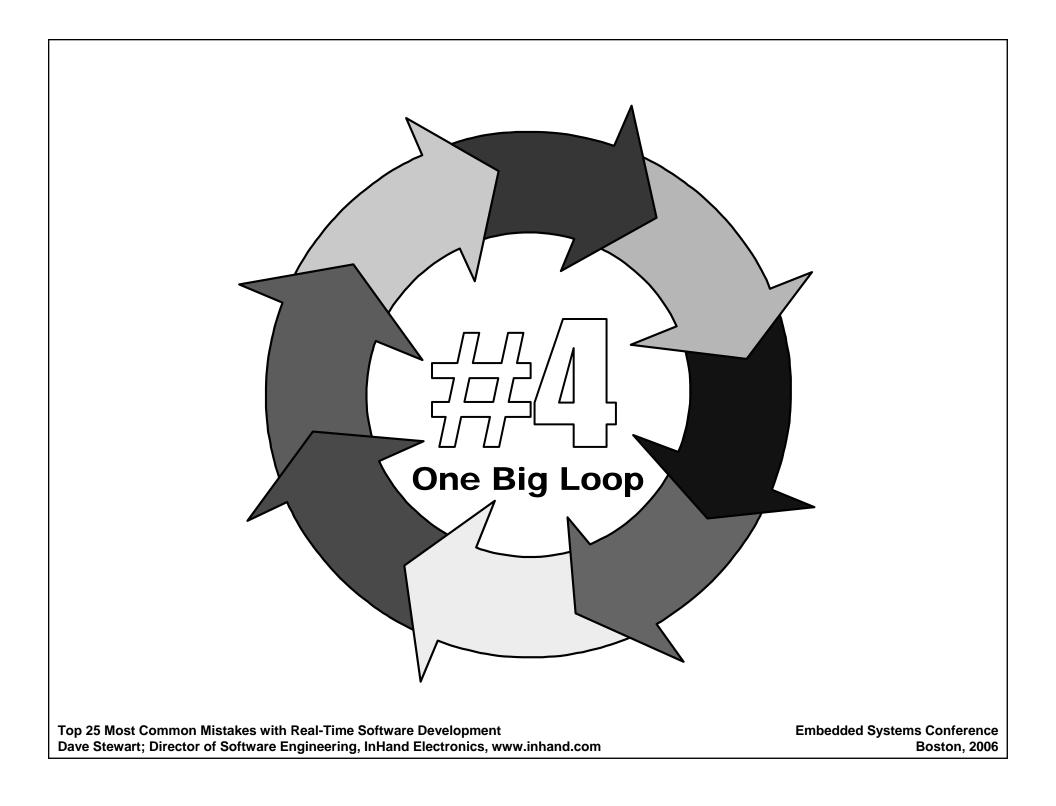


"Nobody else here can help me" syndrome

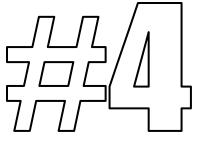


Learn by teaching others!

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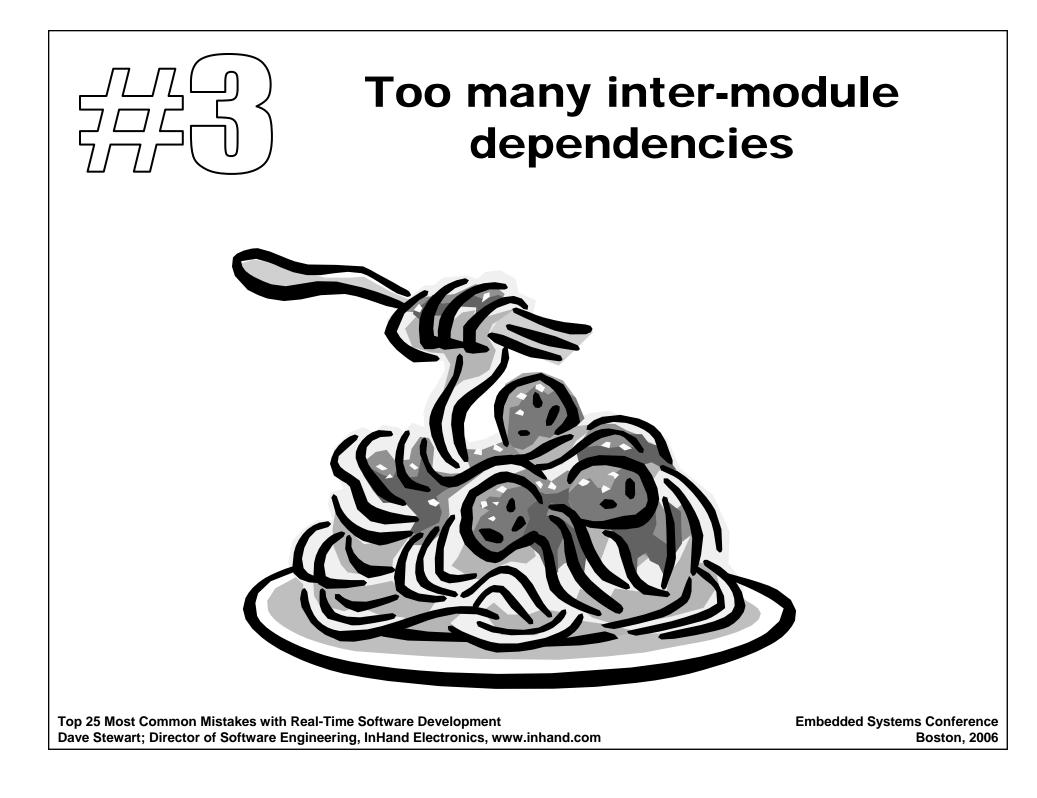
Use proper concurrent design techniques: Non-preemptive: cyclic or multi-rate executive Preemptive: real-time operating system



One Big Loop

Don't use interrupts to emulate multitasking

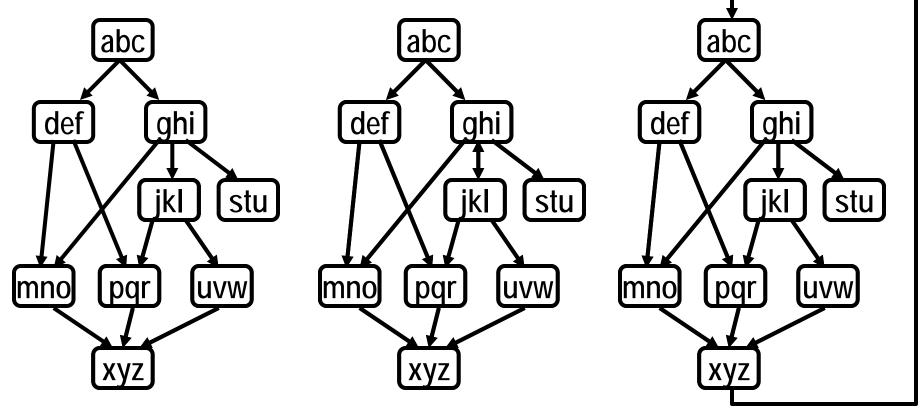
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Too many inter-module dependencies

Example of Dependency Graph



Minimize Circular Dependencies!

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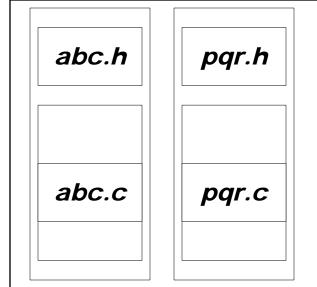


Too many inter-module dependencies

#include "globals.h" problem

Follow fundamental Software Engineering concepts, especially:

- Data encapsulation and modularity
 - Use abstract data types or objects



Hints for maximizing modularity:

Put code for module abc in file abc.c.

Only put definitions of anything exported from abc.c into file abc.h

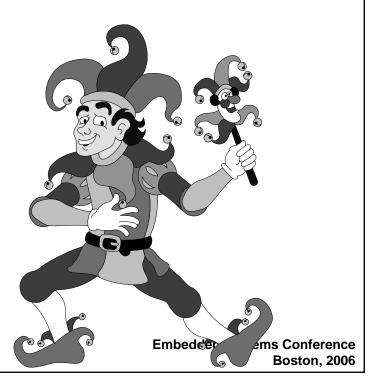
#include only the .h files you need.

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Establish a set of conventions, and stick to them!

Use the conventions to help reader to quickly identify the origin and purpose of the symbol.

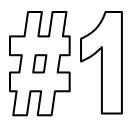


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No measurements of execution time!

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First, design your system so that the code is measurable! Measure execution time as part of your standard testing. Do not only test the functionality of the code!

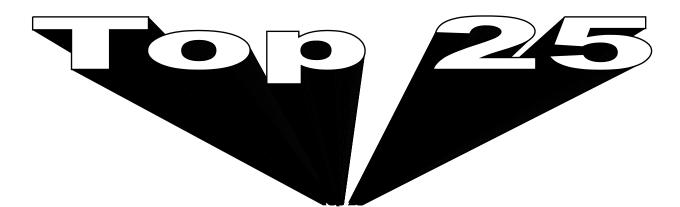
Learn both coarse-grain and fine-grain techniques to measure execution time.

Use coarse-grain measurements for analyzing real-time properties

Use fine-grain measurements for optimizing and fine-tuning

No measurements of execution time!

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Most Common Mistakes with Real-Time Software Development Summary Correcting just ONE mistake can save thousands of dollars or significantly improve quality and robustness of software.

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