4 Realization of Combinatorial Logic

Student Group

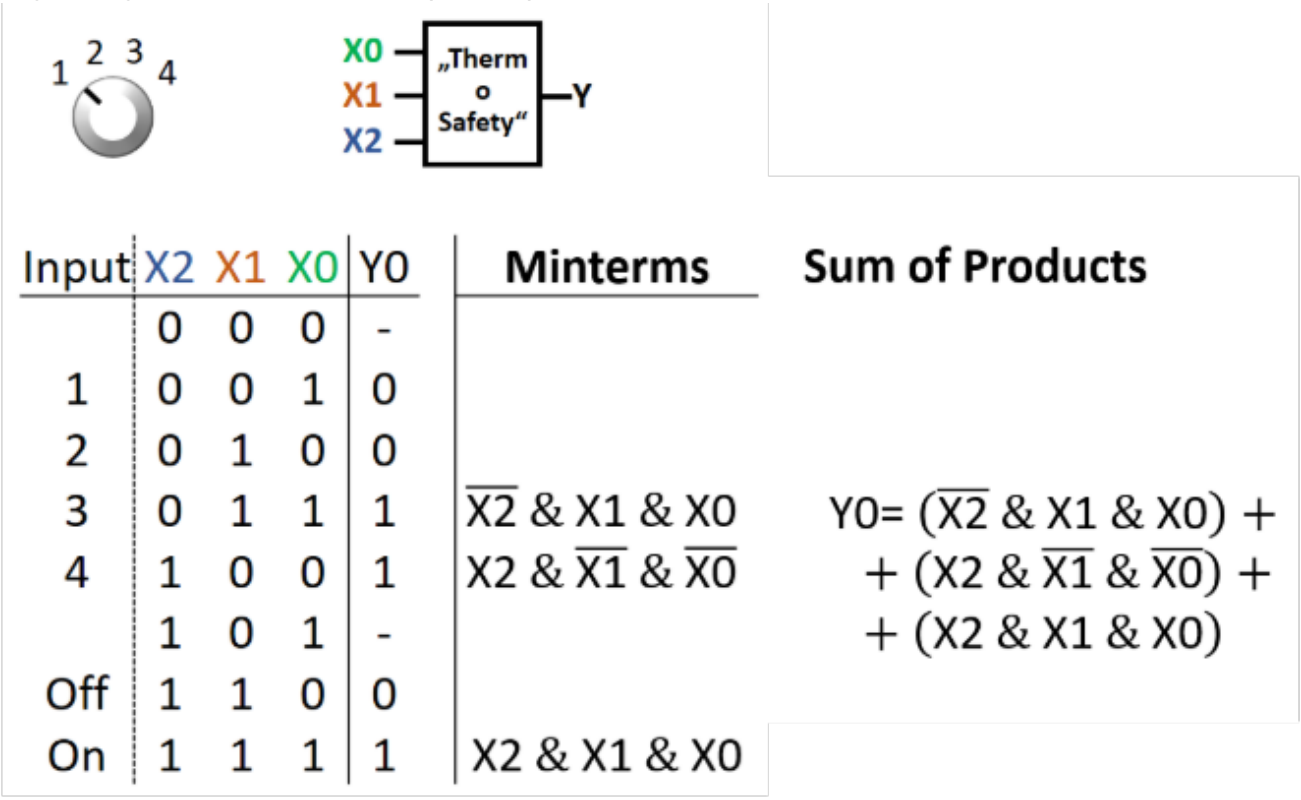
First Name	Surname	Matrikel Nr.

Table of Contents

Realization of Combinatorical Logic

In the last chapter we investigated the Therm-o-Safety example. From this, it was possible to create the logic formula via sum of products of products of sums (see figure 1).

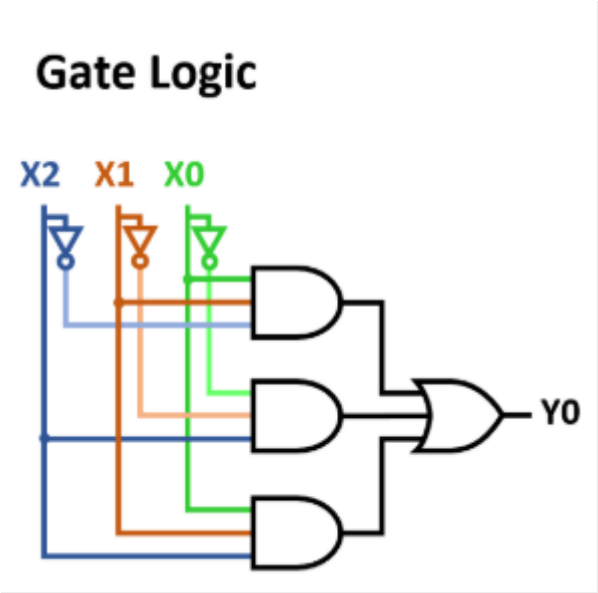
Fig. 1: gate logic from Therm-o-Safety example: Formula



Input	X2	X1	X0	Y0	Minterms	Sum of Products
	0	0	0	-		
1	0	0	1	0		
2	0	1	0	0		
3	0	1	1	1	$\overline{X2}$ & X1 & X0	$Y0 = (\overline{X2}$ & X1 & X0) +
4	1	0	0	1	X2 & $\overline{X1}$ & $\overline{X0}$	+ (X2 & $\overline{X1}$ & $\overline{X0}$) +
	1	0	1	-		+ (X2 & X1 & X0)
Off	1	1	0	0		
On	1	1	1	1	X2 & X1 & X0	

It is simple to derive the gate logic from the formula (figure 2). For each of the three (min)terms an AND-gate combines the needed inputs. As shown in the image, usually parallel to the inputs also the inverted inputs are drawn.

Fig. 2: gate logic from Therm-o-Safety example: Gate Logic



The main question is now: which generalization of the shown logic can be found?

History of the Logic Families

Fig. 3: (historical) Logic Families

Family	Type	Voltage Supply in V	Power Loss per Gate at 100kHz in mW	Power Loss per Gate at 1Mhz in mW	Typical delay time in ns
TTL	7400	5	10	10	10
	74LS00	5	2	2	10
	74S00	5	19	19	3
	74ALS00	5	1	1	4
	74F00	5	4	4	3
	74FS00	5	10	10	1,5
ECL	10.100	-5,2	35	35	2
CMOS	4.000/74C00	5	0,3	3	90
	74HC00	5	0,5	5	10
	74AC00	5	0,8	8	3
	74LVC00	5	0,0001	0,0004	3
		1,8	0,00002	0,00006	6

Fig. ##: Simulation of an Inverter