4 Realization of Combinatorial Logic

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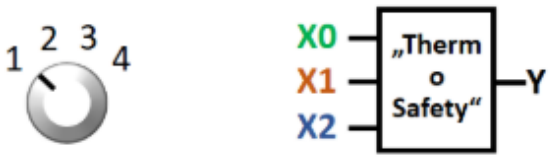
In the last chapter we investigated the Therm-o-Safety example. From this, it was possible to create the logic formula via sum of products of products of sums (see figure 1).

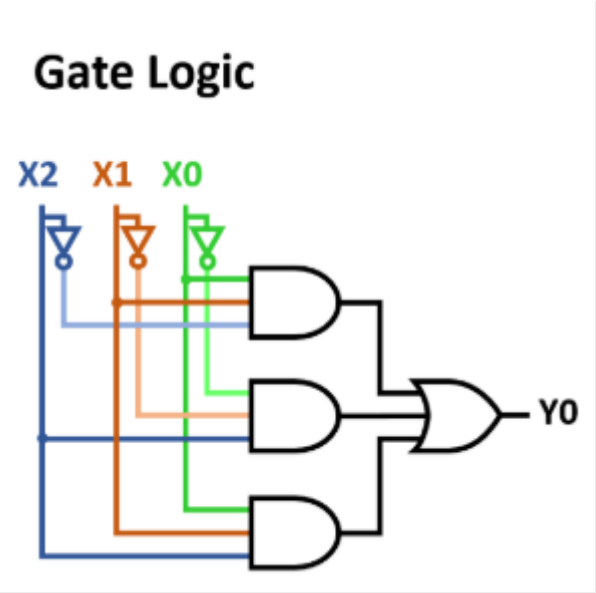
Fig. 1: gate logic from Therm-o-Safety example: Formula



Input	X2	X1	X0	Y0	Minterms	Sum of Products
	0	0	0	-		
1	0	0	1	0		
2	0	1	0	0		
3	0	1	1	1	$\overline{X2}$ & X1 & X0	$Y0 = (\overline{X2}$ & X1 & X0) +
4	1	0	0	1	X2 & $\overline{X1}$ & $\overline{X0}$	+ (X2 & $\overline{X1}$ & $\overline{X0}$) +
	1	0	1	-		+ (X2 & X1 & X0)
Off	1	1	0	0		
On	1	1	1	1	X2 & X1 & X0	

It is simple to derive the gate logic from the formula (figure 2). For each of the three (min)terms an AND-gate combines the needed inputs. As shown in the image, usually parallel to the inputs also the inverted inputs are drawn.

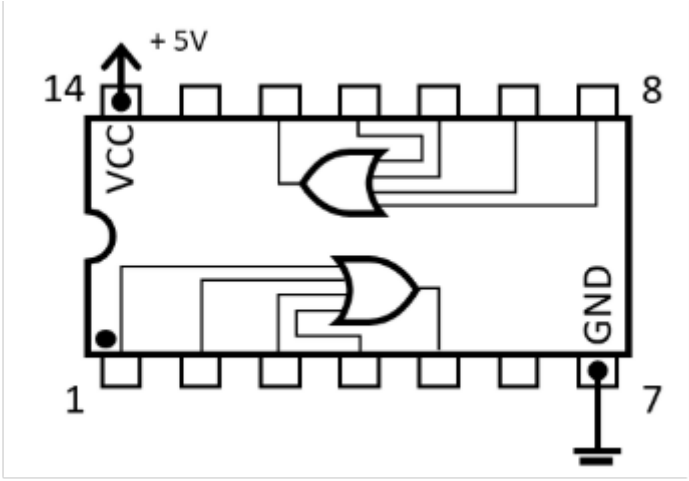
Fig. 2: gate logic from Therm-o-Safety example: Gate Logic



The main question is now: which generalization of the shown logic can be found?

History of the Logic Families

A huge variety of integrated circuits (ICs) were used historically. figure 3 shows two separate integrated circuits: There can be single or multiple gates in an IC with two or more inputs. The most used IC series was the 74xx ICs, where the xx are numbers which define the internal logic.



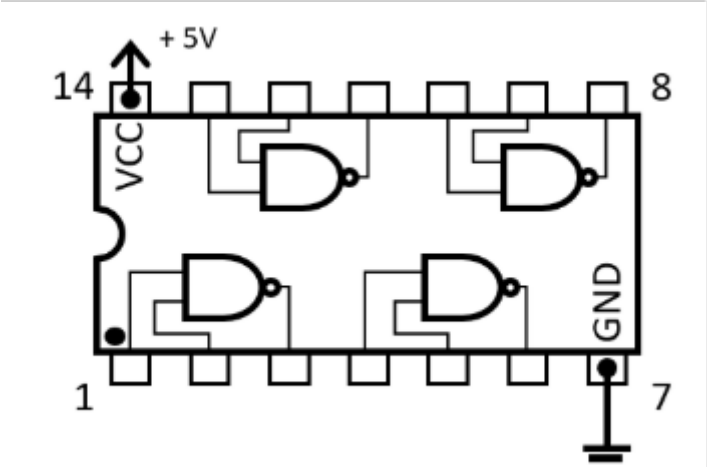


Fig. 3: integrated circuit

The logic families which were first developed were based on bipolar transistors. To use these as an closed switch a constant current is needed. This result in relatively high power losses. Depending on the combination of these transistors this logic families were called “transistor transistor logic” (TTL) or “emitter coupled logic” (ECL). The name TTL survived as a designation for the needed voltage levels $0V$ and $5V$. The $5V$ can still be found as supply voltage in some logic circuits.

Modern controller an logic is based on CMOS. figure 4 shows that this type of logic only disipates a fraction of the energy loss (and therefore heat) compared to the older logic families. This started the logic circuit develompent, which lead to mobile phones, computer and all the other present digital controller.

The 74xx series is nowadays mostly from historical interest. Nearly all of the applications can now be done directly with microcontrollers. In rare cases they are still used as “glue logic” between two logic ICs, e.g. as for adjusting the logic voltage level.

Fig. 4: (historical) Logic Families

Family	Type	Voltage Supply in V	Power Loss per Gate at 100kHz in mW	Power Loss per Gate at 1Mhz in mW	Typical delay time in ns
TTL	7400	5	10	10	10
	74LS00	5	2	2	10
	74S00	5	19	19	3
	74ALS00	5	1	1	4
	74F00	5	4	4	3
	74FS00	5	10	10	1,5
ECL	10.100	-5,2	35	35	2
CMOS	4.000/74C00	5	0,3	3	90
	74HC00	5	0,5	5	10
	74AC00	5	0,8	8	3
	74LVC00	5	0,0001	0,0004	3
		1,8	0,00002	0,00006	6

Logic Stages

From the <img pic02> we know how the logic for the sum of products looks like. in figure 5 also the gate logic for the product of sums is shown. Both consist of two logic stages:

- For sum of products the first logic stage are the OR-gates, the second stage is the AND-gate,
- For product of sums, it is just the other way around: first logic stage AND-gates, second stage OR-gate.

Generally, the two-stage setup allows to implement any possible logic based on a truth table.

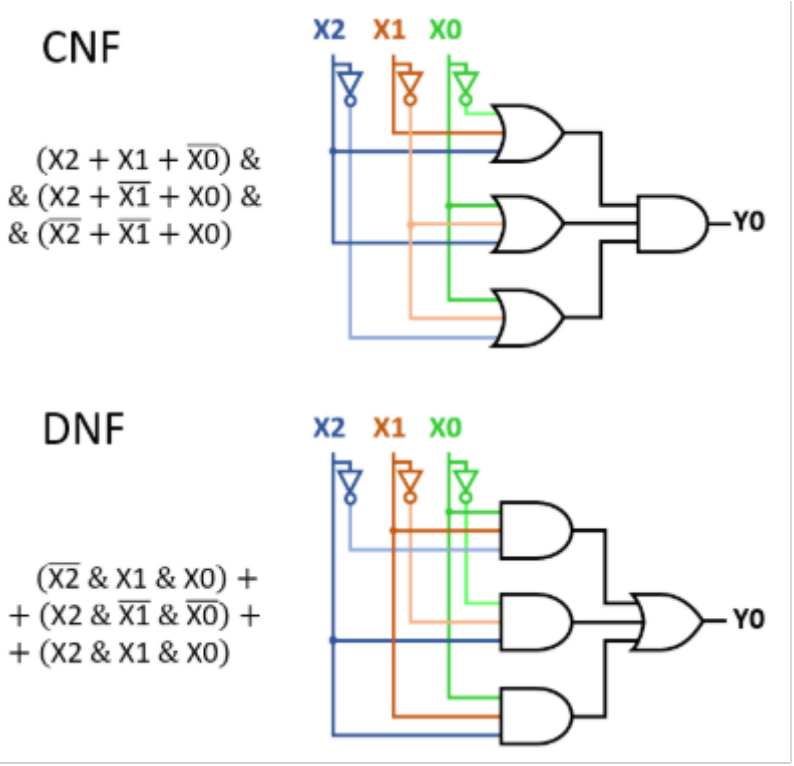
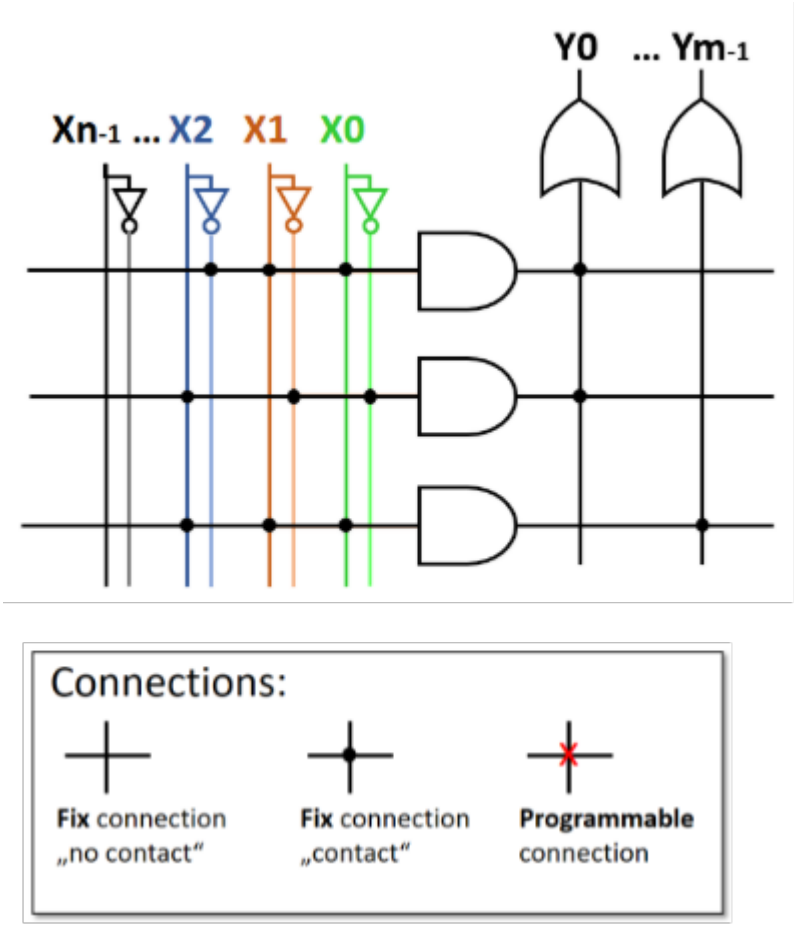


Fig. 5: Logic Stages

Often a simplification of the circuit represenation is used. There the multiple input ant output lines are

reduced to one single line, representing a bus (= multiple parallel lines). Only the inputs which where the crossing of the lines are marked with a black dot are used as an input for the stages. These connections are fixed. Often also programmable connections are used, wich are usually set during production. The logic stages can be seen in figure 6.

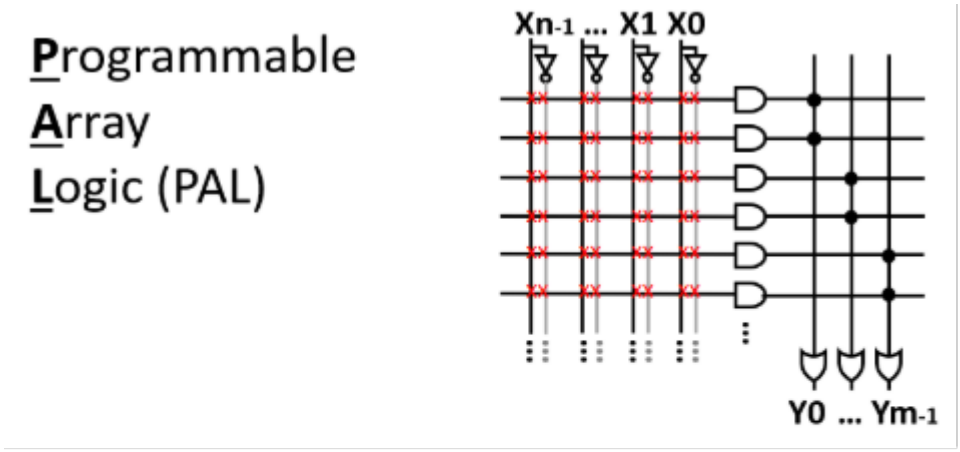
Fig. 6: simplified representation of the stages

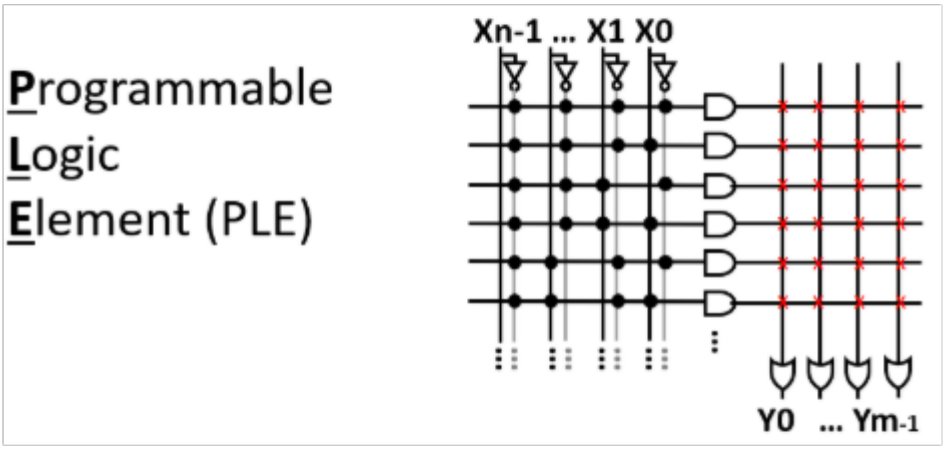


When there are programmable connections, the IC is called programmable logic device (PLD). Depending on the position of the programmable connections, these PLDs are separated into (see figure 7):

1. Programmable Array Logic (PAL): first stage is programmable, second stage is fixed
2. Programmable Logic Element (PLE): first stage is fixed, second stage is programmable
3. Programmable Logic Array (PLA): both stages are programmable

Fig. 7: different types of PLDs





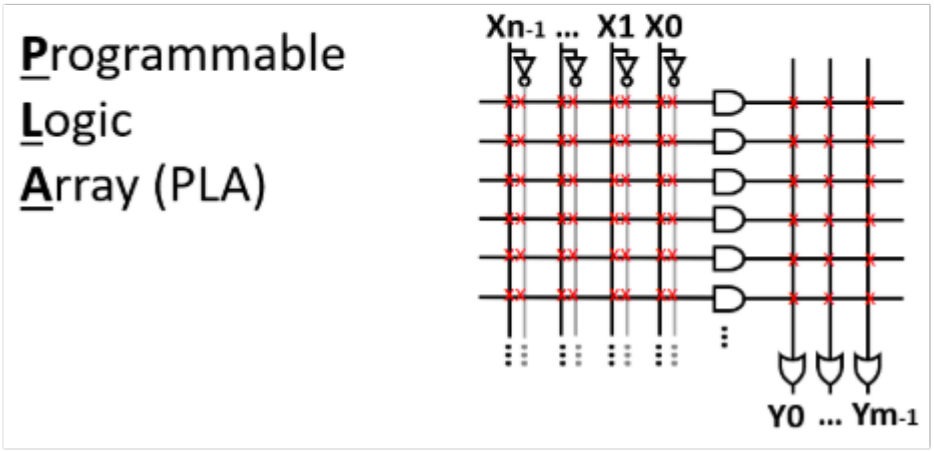


Fig. ##: Simulation of a PAL

Fig. ##: Simulation of a PLE