

5 Storage Elements

Student Group

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5. Storage Elements

In the previous chapter we have had a look onto memory devices, which store data even when no voltage is applied. This is great for longterm storage, like measurement data, pictures or music. The clock frequency of the storage element are often much lower than the internal frequency of the processor / controller. By this, the processor has to wait for the stored information due to high access time.

Therefore an controller-internal memory is advantageous. These are often called cache. Distinct storage elements have special properties, e.g. the written data changes the logic level of a pin ('foot') of the IC directly. We will now focus onto these controller-internal, fast memory, which consist of logic gates.

The name flipflop stems from the fact, that the smallest logic circuit for storing data has to store binary values. Therefore, it has to show one of two stable states, and can flip into the other one by an external interaction.

5.1 Flipflop as a Blackbox

In order to understand the wanted storage element, we will first look onto these element based on the IPO model (input-process-output).

The process of the storage element is to store two different states. This property can be implemented via two inverting gates which are interconnected in a feedback loop. The simple setup would be with NOT gates as shown in [figure 1](#).

Fig. 1: Storing two different states

Of course this simple elements misses inputs and outputs! Therefore we have to look into these now.

The input of this element needs at least two inputs. Often the following two are used:

- Set input: once this input is high, a 1 is stored. This input is marked as S .
- Reset input: once this input is low, a 0 is stored. This input is marked as R .

For the output also often two pins are shown. The pin Q outputs the stored data directly. The pin \bar{Q} outputs the inverted value.

Based on this simple requirements we can create the truth table:

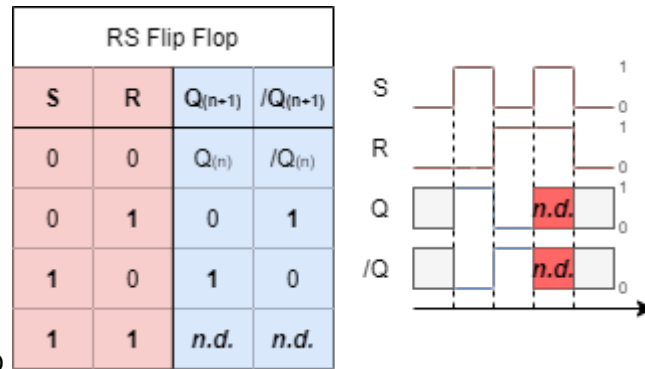


Fig. 2: truth table for flipflop

In [figure 2](#) the last input ($S=1$, $R=1$) reaches a not defined state.

Examples

Fig. ##: Shift Register with synchronous Load

Fig. 31: Shift Register with synchronous Load, Direction Bit and Sout

further Links

- https://www.electronics-tutorials.ws/sequential/seq_1.html
- https://www.electronics-tutorials.ws/counter/count_1.html

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